REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application. Claims 7-9 and 17-18 have been withdrawn and claim 21 has been amended based on Fig. 4 of the original drawings. Accordingly, claims 1, 5, 6, 12-16 and 19-23 are presently under consideration.

Claims 21 and 23 are objected to because of informalites. Claims 21-22 are rejected under 35 USC 102(e) as being anticipated by Moon et al. (US 2004/0095303, hereinafter "Moon"). Claims 21-22 are rejected under 35 USC 102(b) as being anticipated by Kawaguchi (US 6,052,171, hereinafter 'Kawaguchi"). Claims 1, 5-6, and 12-16 are rejected under 35 USC 103(a) as being unpatentable over Moon in view Kim et al. (KR 10-1999-0024956, hereinafter "Kim"). Claims 19-20 are rejected under 35 USC 103(a) as being unpatentable over Moon in view of Kim; further in view of Song et al. (US 2002/0008794, hereinafter "Song"). Claims 1, 5-6, and 12-16 are rejected under 35 USC 103(a) as being unpatentable over Kawaguchi in view of Kim. Claims 19-20 are rejected under 35 USC 103(a) as being unpatentable over Kawaguchi in view of Kim; further in view of Song. Claim 23 is rejected under 35 USC 103(a) as being unpatentable over Kawaguchi or Moon in view of Song. These rejections are respectfully traversed.

As the Examiner will note, claim 21 has been amended to recite the feature wherein the common voltage line is adjacent to <u>both</u> the gate pad and the data pad." (Emphasis added) Accordingly, claims 21 and 23 now correspond to Fig. 4 and the present application. Accordingly, it is believed that the objections to claims 21 and 23 have been eliminated.

It is the Applicants' position that the Moon (US 2004/0095303) reference is not available as prior art against the present application. The present application claims the benefit of foreign priority to Korean Patent Application No. 2002-0078376 which was filed on December 10, 2002. However, the Moon reference was filed in the United States on July 9, 2003, (that is, after the priority date of December 10, 2002). Therefore, Moon is not available as prior art against the present application. A verified English translation of the priority document will be filed in the USPTO subsequent to the filing of the present Amendment. Therefore, it is believed that the rejections relying upon the Moon reference should be withdrawn.

In the Examiner's Response to Amendment on page 2 of the Office Action the Examiner mentions that Figure 1A of Kawaguchi just shows a portion of the peripheral part of the liquid crystal panel. Therefore, when a full peripheral part is shown, the first and second line-on- glass signal lines and pads should be in between the first gate pad and the first data pad. Further, the Office Action at page 5 mentions that Kawaguchi discloses in Col. 6, lines 60-65 a plurality of line-on glass type signal lines as connection line 13. However, these arguments are respectfully traversed. In Fig. 1A of Kawaguchi, the peripheral part 15 is one side of liquid crystal panel 10. That is, the peripheral part 15 corresponds to source line 11 and an upper side or a lower side of quadrilateral liquid crystal panel 10. **There is no evidence that the peripheral part 15 is disposed in one corner of the liquid crystal panel 10 in Kawaguchi.**

Fig. 1A

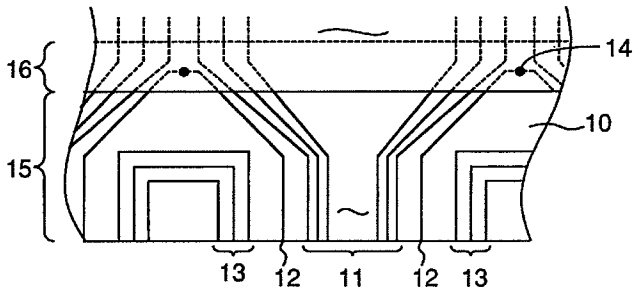
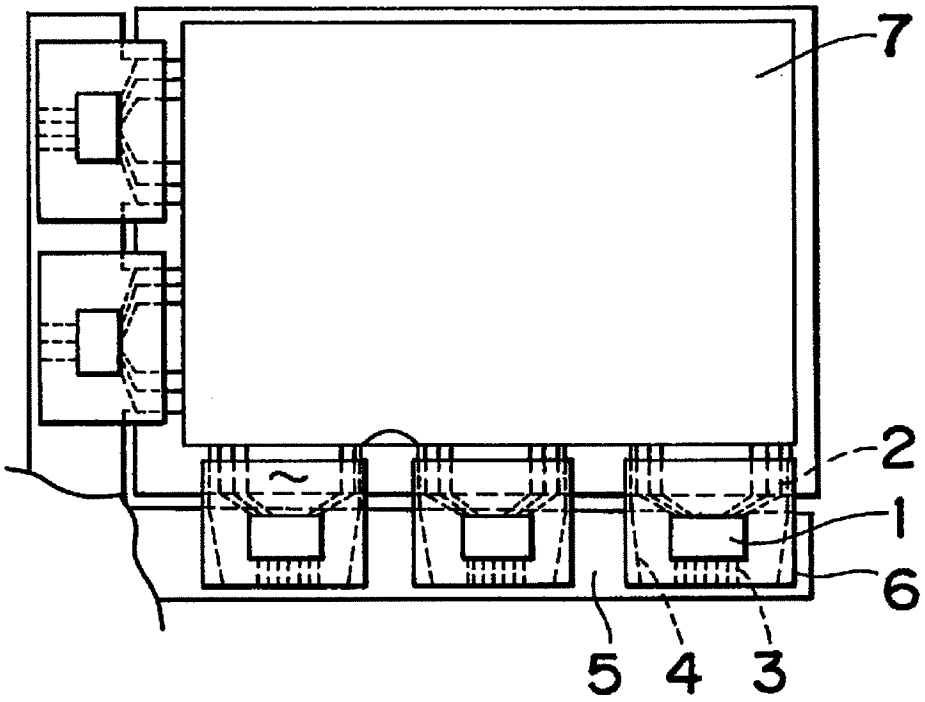


Fig. 1A~1C of Kawaguchi show TCP and its connection with liquid crystal panel 10 and circuit board 30. The TCPs 6 are formed in a lower side of the liquid crystal panel 10 and not in one corner between the first gate pad and the first data pad. Please see Fig. 5 of Kawaguchi.

Therefore, the shown peripheral part of Fig. 1A is just one side of liquid crystal panel 10.

Fig. 5 PRIOR ART



In column 6, lines 60~65, Kawaguchi mentions that the embodiment is applicable also to the gate line side, and similar effects can be obtained. Herein, the gate line side corresponds to the left side or right side of the liquid crystal panel 10, not the one corner between the first gate pad and the first data pad. Thus, Kawaguchi does not teach or suggest the possibility of lines or pads in one corner defined between the first gate pad and the first data pad.

Accordingly, Kawaguchi does not disclose the following features:

"a plurality of first line-on glass signal pads formed just beside the first data pad and a plurality of second line-on glass signal pads formed just beside the first gate pad, the first and second line-on glass signals pads are in one corner of the outer area of the picture display part,

wherein the one corner of the outer area of picture display part is defined between the first gate pad and the first data pad;,"

"a plurality of line-on glass type signal lines connecting the first and second line-on glass signal pads in the corner of the outer area of the picture display part for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;,"

"a plurality of first dummy pads between the first line-on glass type signal pads and a plurality of second dummy pads between the second line-on glass type signal pads;" and

"a plurality of dummy lines connecting the first and second dummy pads in the one corner of the outer area of the picture display part, wherein the plurality of first and second dummy lines are formed between the line-on glass type signal lines for applying a common voltage as a reference voltage to drive the liquid crystal cells with at least one layer of insulating film therebetween, wherein the insulating film covers the plurality of line-on glass type signal lines and the dummy lines are formed on the layer of insulating film" (emphasis added) as recited in claim 1 of the present application.

Also, the Kim and Song references fail to show the above features. Accordingly, none of the cited references including Kawaguchi, Kim and Song teaches the above features of the present invention. Thus, the Applicant respectfully submits that claim 1 and claims 5-6, which depend therefrom, are allowable over the cited references.

Similarly, for the same reasons, claim 12 is allowable over Kawaguchi and Kim in that claim 12 recites the features, for example, "forming first~ (n)th gate lines in a picture display part and a plurality of line-on glass signal lines in one corner of an outer area of the picture display part on a substrate for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;

forming at least one layer of insulating film to cover the line-on glass type signal lines;

forming first~(m)th data lines to cross the first~ (n)th gate lines in a picture display part and a dummy line that is located between the line-on glass signal lines on the insulating film for applying a common voltage as a reference voltage; and

forming first~(m)th data pads extended from the first~(m)th data lines and first~ (n)th gate pads extended from the first~ (n)th gate lines in the outer of the picture display part and forming first and second line-on glass signal pads just beside the first data pad and first gate pad, respectively and first dummy pads between the first line-on glass signal pads and second dummy pads between the second line-on glass pads, respectively, in one corner of the outer area of the picture display part, wherein the one corner of the outer area of picture display part is defined between the first gate pad and the first data pad,

wherein each of the plurality of the line-on glass signal lines is connected between the first and the second line-on glass signal pads in the one corner of the outer area of the picture display part." (Emphasis Added)

As stated above, none of the cited references, singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 12 and claims 13-16, which depend from claim 12 are allowable over the cited references.

Claim 19 is allowable over Kawaguchi, Kim and Song in that claim 19 recites, for example, the following features,

"a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one corner of the outer area of the picture display part is corresponding to between the gate pad and the data pad;

an insulating layer covering the line-on glass type signal lines; and

a plurality of common voltage signal lines for applying a common voltage signal and being formed between line-on glass type signal lines, on the insulating layer,

wherein at least one of the plurality of common voltage lines applies the common voltage signal through a silver(Ag) dot to a common electrode that is formed on an entire surface of an upper substrate" in the claimed invention. (Emphasis added)

Therefore, none of the cited references including Kawaguchi, Kim and Song, singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly,

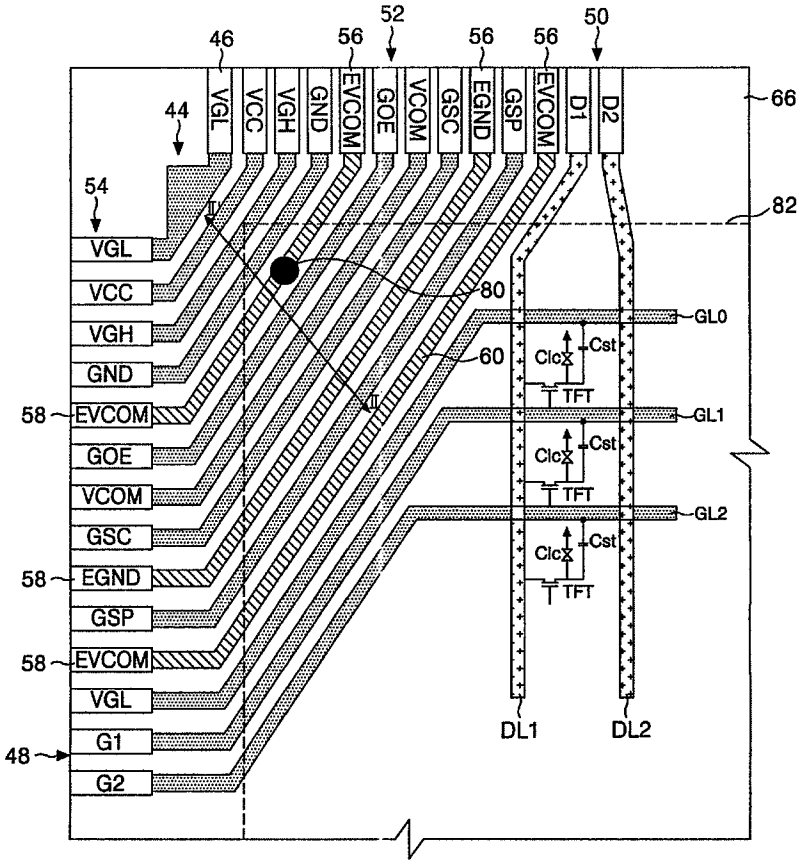
the Applicant respectfully submits that claim 19 and claim 20 which depends from claim 19 are allowable over the cited references.

Claim 21 is allowable over Kawaguchi, Kim and Song in that claim 21 recites the features:

"a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate for applying drive gate signals to drive the liquid crystal cells, wherein the one corner is defined between the gate pad and the data pad;" and

"a common voltage line located in the one corner, wherein the common voltage line is adjacent to both the gate pad and the data pad."

In the claimed invention, since the common voltage line is adjacent to the both the gate pad and the data pad (please see Fig. 4, as shown the below), resistance of common voltage between the gate pad and the data pad can be reduced and delay of common voltage can be reduced. Therefore, deterioration of the image based on a drop of common voltage can be prevented.



None of the cited references Kawaguchi, Kim and Song, either singly or in combination, teaches or suggests at least these features of the present invention. Thus, the Applicant respectfully submits that claim 21 and claims 22-23 which depend from claim 21 are allowable over the cited references.

In view of the above amendments and remarks, reconsideration of the rejections and allowance of all the claims of the present application are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Joseph A. Kolasch, Registration No. 22463 at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: May 3, 2010

Respectfully submitted,

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